A GaAs MONOLITHIC PHASE SHIFTER FOR 30 GHZ APPLICATION*

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Abstract

The design and performance of a GaAs monolithic 180° one-bit phase shifter test circuit for Ka-band operation is presented. Over the 27.5 to 30 GHz band the measured differential phase shift is within 10° of the ideal characteristic and the insertion loss is between 4 and 6 dB. The switching FETs are fabricated by ion implantation into LEC material using a power FET implant schedule. I-V characteristics are also presented for a self-aligned gate FET whose channel resistance is reduced by more than a factor of two relative to the power FET. This latter fabrication technique holds promise in reducing phase shifter insertion loss for mm-wave applications.

Introduction

As GaAs monolithic technology progresses to higher frequencies, it becomes natural to consider the development of specific integrated circuit functions which are required by potential millimeter-wave system applications. The applications that take greatest advantage of monolithic circuit implementation include phased array systems for communications and radar where a large number of small low cost circuits are needed. For such systems an essential circuit function is phase shifting at the carrier frequency. This paper presents some recent results on a one-bit 180° phase shifter test circuit in Ka-Band. Specifically the work is aimed at potential application in a phased array satellite receiver operating in the 27.5 to 30 GHz band. Because of the receiver application, consideration is made for small signal operation only. The monolithic GaAs chip incorporates passive switching FETs and microstrip transmission lines. The use of passive FETs is vital for low dc power consumption. The FETs are fabricated by direct ion implantation into undoped LEC material, while the microstrip transmission lines are formed on the semi-insulating substrate. Two approaches to switch fabrication are being pursued: A conventional power FET approach and a self-aligned gate technique which holds promise for reducing resistive parasitics in the switching FETs. The latter is especially important for mm-wave circuits.

Design Considerations

The design of the 180°-bit test circuit is based on a switched transmission line type of configuration using switching FETs to RF switch between two microstrip lines. The differential electrical length of these lines is equal to 180° at center band, i.e., phase shifting is accomplished by true time delay. The FETs are passive in the sense that no dc bias is applied to the drain and only a switching voltage (0,-6v) is used at the gate [1-3]. For broad bandwidth and low sensitivity to variations in device parameters, the circuit utilizes a pair of SPDT switches realized by four, 300 micron gate-width FETs in shunt across the 50 Ω transmission lines with each FET located at a distance of $\lambda g/4$ (0.8 mm at 30 GHz on GaAs) from either the input or output Tee-junction. The circuit layout, shown in Figure 1, is conservative in that the area required (chip dimensions are 3 x 2.67 x 0.2 mm^3) has not been minimized. This was done to ensure that the coupling between adjacent sections of transmission lines would be negligible thereby facilitating evaluation of initial RF performance results. The 0.2 mm substrate thickness was chosen as a compromise between increased microstrip transmission line loss and extraneous capacitive parasitics (thinner substrate), versus increased circuit layout dimensions (thicker substrate). Since the circuit is passive, heat sinking of active elements is not an issue and a relatively thick substrate can be used. As shown in Figure 1,

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pads are provided at the edge of the chip for grounding. For these tests ground connection is accomplished by a series resonant circuit consisting of an external 0.1 pF capacitor (bottom plate soldered to ground) and a mesh wire inductor connecting from the capacitor top plate to the grounding pad on the chip. To increase the high impedance state (V_g = -6V), a short section of 90 Ω line is used to resonate the pinch off capacitance between drain and source (C = .07 pF) for each FET.

An important design consideration is the dissipative loss associated with the switches and the microstrip lines. As shown in the following the dominant losses occur in the passive FETs. Microstrip line loss is calculated to be about 0.15 dB per wavelength at 30 GHz based on metal losses only and a gold thickness of 1.5 microns for a 50 Ω line on 0.2 mm thick semi-insulating GaAs [4]. Experimentally, RF line losses measured at 30 GHz on GaAs as well as on sapphire substrates (of the same thickness) indicate comparable performance.

For the switching FETs, however, RF losses are primarily associated with the resistances in the channel; the "open" channel resistance, R_{on}, for the case of the low impedance state (V_g=0), and r_s, the residual series resistance in the pinched-off channel ($V_g \cong$ -6V) [2]. The effective "off" resistance, R_{off}, at resonance, i.e., when the pinch-off capacitance is resonant with the external inductance, is approximately equal to, $R_{off} = r_s Q^2$, where $Q = (\omega r_s C)^{-1}$. For a typical 300 micron power FET R_{on} = 11-14 Ω and with C = 0.07 pF, and $r_s \cong 5\,\Omega$, R_{off} is about 1000 Ω at 30 GHz. By choosing these ON and OFF resistance values and using them in an ideal SPDT switch configuration as shown in the inset of Figure 2 we can calculate the ideal insertion loss and isolation of a single switch at center frequency. Furthermore, by scaling R_{on}, r_s, and C for other gatewidths an estimate can be made of the required gate width to be used to obtain high isolation and low insertion loss. It is also necessary to consider the size of the FET layout relative to the guide wavelength. This is shown in the curves of Figure 2 calculated for 30 GHz operation. A reasonable trade-off between good isolation and high insertion loss versus large layout dimensions relative to a wavelength is to choose a 300 or 400 micron gate-width FET. Note that even for the ideal case where only dissipation in the device resistances are considered, a loss of about 1.1 dB per switch or 2.2 dB per bit for a phase shifter circuit, is predicted.

To minimize these losses it is essential to reduce the channel parasitic resistances. One approach is to use a self aligned gate technique which has the potential for reducing these parasitics.

Device Fabrication

Two processes have been used for fabricating switches: one process uses a standard power FET implant; the second uses a self-aligned gate process. The power FET approach uses standard GaAs FET processing including silicon ion implantation for the channel region, mesa etching for device isolation, a Au/Ge/Ni ohmic contact, and a recess etch for the gate. A Ti/Au overlay is used for microstrip circuit and pad metal. FETs fabricated by this approach have a DC ON resistance of 11-14 ohms.

The self-aligned gate process is an approach that has been primarily used for digital IC's [5]. This process offers the advantage of lower ON resistance than the power FET switch. The self-aligned gate allows a low sheet resistance N^+ implant to be brought up very close to the gate thereby minimizing the resistance of material in the gate-source and gate-drain regions. The refractory metal gate is made of Ti/W silicide which can withstand the subsequent high temperature implant anneal. The first implant anneal is done at 850 °C after the channel implant for good activation, the second anneal is done at 800 °C after the N^+ implant. The lower temperature for the second anneal allows reasonable N^+ activation while minimizing diffusion of the gate metal. Ohmic level metal is applied and sintered after the second implant anneal.

The gate level metal is defined by an etch technique. Undercutting during the gate metal etch leaves a resist overhang which serves as an implant mask and separates the N^+region from the gate. This technique gives self-aligned gate switches with reasonable gate breakdown voltages

The TiW silicide gate metallization has a higher resistivity than the metals normally used for low noise and power FETs. However, the gate resistance is not as critical for the present application since no RF signal is applied to the gate.

Experimental Results and Comparison With Computer Calculations

To interface the phase shifter chip with standard Ka-Band circuitry a test fixture having WR-28 waveguide input and output ports is used. Antipodal fin-line transitions fabricated on 0.25mm thick RT/duroid are employed to transition from waveguide to microstrip [5-6]. Typical insertion loss for a pair of back to back transitions including a 2.5 cm length of connecting 50 Ω microstrip line is 0.6 to 0.8 dB from 26.5 to 37 GHz. A photograph of the test fixture with the cover removed is shown in Figure 3.

RF measurements of differential phase and insertion loss were performed on a network analyzer using the H.P. 26-40 GHz waveguide reflection - transmission test set. A scalar reflectometer test set was also used to measure insertion loss and return loss.

Figure 4 shows the measured differential phase shift from 27.5 to 32.5 GHz. Over the band of interest, 27.5-30 GHz, the measured phase shift is within 10° of the ideal time delay characteristic, i.e., a slope of 6°/GHz. Note that beyond 30 GHz the measured differential phase changes slope and begins to decrease. Computer calculations of the phase shifter circuit based on a simple model similar to that used in Reference [2] or [3] but including parasitic effects, have shown that such a decrease can result because of parasitic shunt capacitance, C_p, loading the transmission line. Specifically, it was found that the metallization pattern of each FET contributes about 0.1 pF of shunt capacitance to ground and when included in the calculations, a change of slope for the differential phase does indeed occur beyond 30 GHz. It is important, therefore, to minimize shunt capacitance by incorporating the FET into the transmission line as much as possible (via holes, if practical in a 0.2mm thick substrate, would help), or to increase the substrate thickness. Extraneous shunt capacitance also increases the insertion loss as discussed below.

Calculated values of the phase shifter insertion loss (when transmission line losses and the parasitic, C_p, capacitances of the FET layout metallization are included) lie between 3 and 5.0 dB across the 26-33 GHz band using values of $R_{on} = 14\,\Omega$, $r_s = 5\,\Omega$, $C = 0.07$ pF and $C_p = 0.1$ pF. Measured results lie between 4.2 and 6 dB across the same band. Although the exact cause of this discrepency is not yet known, at least one factor helps explain the difference. Namely, some substrate surface conduction was observed on the wafers on which phase shifter circuits were fabricated. Although mesa etching was used for isolation, increased loss due to surface conduction could still occur in the switching FETs. Such losses would be especially significant in the "ON" branch of the phase shifter when the shunt FETs are in their high impedance state.

As discussed above, the self-aligned gate technology is one approach to reducing the resistive losses in passive FETs. This is an especially important consideration for circuits employing switching FETs at mm-wave frequencies. As of this writing we have fabricated a run of phase shifter circuits using the self-aligned gate technique. Although we have not yet RF-evaluated a phase shifter circuit from this run, a dc I-V characteristic of a 300 micron FET taken from a test pattern area is shown in Figure 5. As seen from the trace of the drain characteristics for $V_g = 0$, the low field resistance corresponding to R_{on}, is less than $6\,\Omega$. This is in contrast to a typical value of 11-14 Ω for a comparable FET having a conventional power FET implant schedule.

Conclusions

Initial results of a 180°, one-bit monolithic phase shifter test circuit for operation in the 27.5-30 GHz band have been presented. Over the band of interest the phase shift versus frequency characteristic is within 10° of the ideal curve.

Although a reasonably good phase shift characteristic is obtained, the losses in the circuit range between 4 and 6 dB and are relatively high for system applications requiring high efficiency such as in satellite borne communication receivers. Computer-simulations based on simple equivalent circuits indicate that the loss is dominated by the resistive dissipation occurring in the channels of the switching FETs, which is especially high at mm-wave frequencies. Extraneous parasitic shunt capacitance associated with the details of the circuit layout also contribute significantly to the total insertion loss of the circuit. The latter can be controlled by careful layout and the use of thicker substrates. An approach to reducing the intrinsic resistive losses in the FET, which is compatible with the phase shifter application, is to make use of a self-aligned gate technology. A reduction in the open channel resistance by more than a factor of two has been demonstrated for a switching FET obtained from a test pattern area of a self-aligned run of phase shifter circuits. This is a promising technology for implementation in switching circuits at mm-wave frequencies as well as for similar applications at lower microwave frequencies.

Acknowledgements

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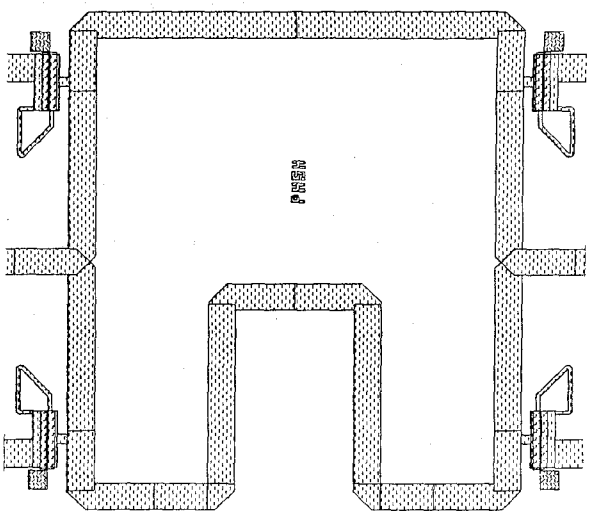


Figure 1. Phase Shifter Circuit Layout

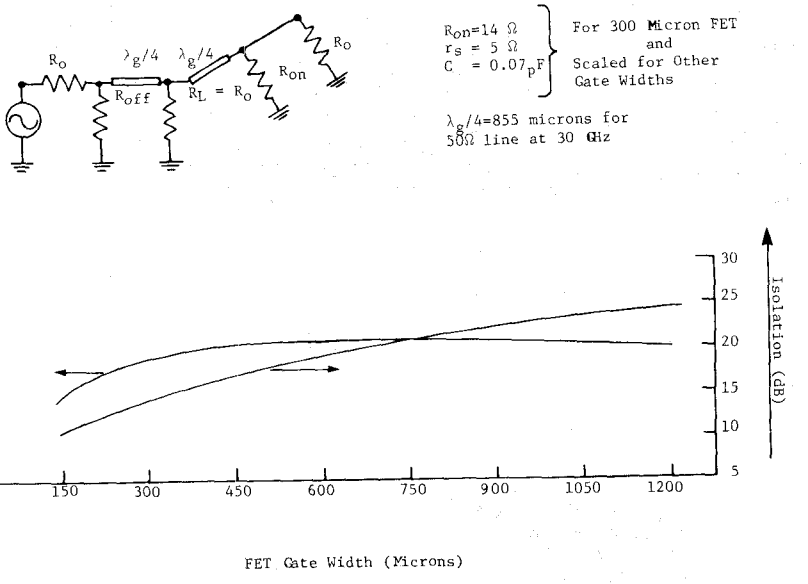


Figure 2. Calculated Insertion Loss and Isolation versus FET Gate Width for Idealized Model

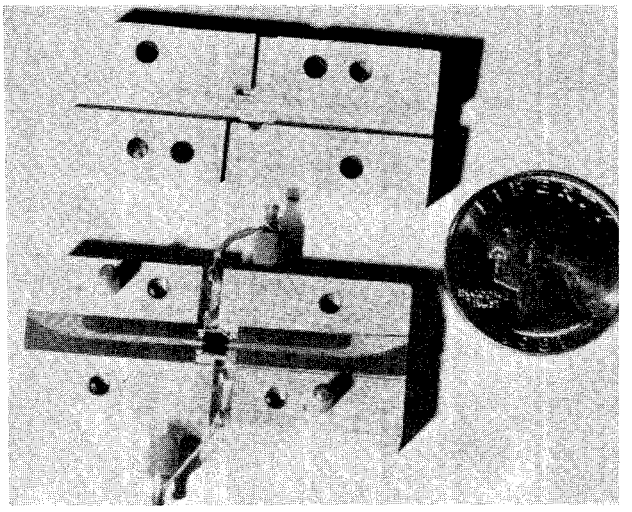
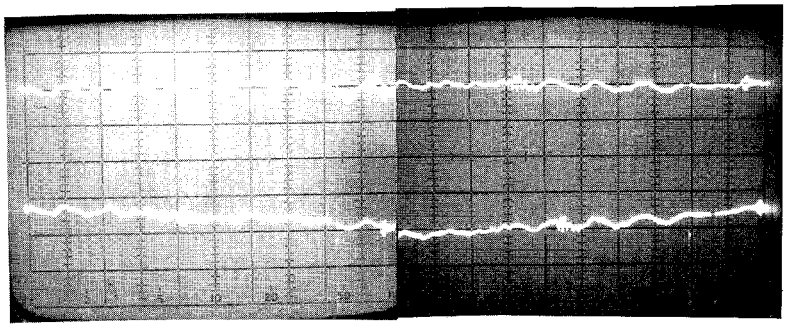


Figure 3. Ka-Band Test Fixture

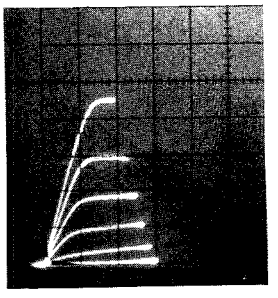


State 1

State 2

Vertical: 45^{o}/div
Horizontal: 250 MHz/div, 27.5-32.5 GHz

Figure 4. Differential Insertion Phase



Vertical : 50mA/div
Horizontal: 1V/div
Gate : 2V/step

Figure 5. I-V Characteristics for a Self-Aligned 300 Micron Gate Width FET